Serial Number: 10/005,895 Filing Date: November 2, 2001

Title: HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

Assignee: Intel Corporation

## **REMARKS**

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-13 and 42-59 are now pending in this application.

# Objection to the Specification

The disclosure was objected to because of the following informalities. Specifically, the Office Action on page 2 states,

Refer to page 3 line 17. What is "3GIO"? Applicant has not responded to the question as to what this acronym stand for and its importance in the context of this invention.

In a previous response submitted to a prior Office Action (the previous response mailed May 26, 2005 in response to the prior Office Action mailed December 28, 2004), Applicant submitted the following reply to this rejection:

The disclosure is objected to because of informalities. Specifically, the Office Action requests a correction/clarification regarding the use of the term "3GIO" at page 3, line 16 of the specification. Applicant directs the Examiner's attention to page 1, lines 14-17 of the specification which states, "Most recently, switching fabric has been used as an interconnection means between the host and the end nodes of a processing domain. Some examples of switching fabric technologies that may be used include 3GIO, Rapid I/O<sup>tm</sup>, and HyperTransport<sup>tm</sup>." Applicant submits that "3GIO" is clearly set forth in the patent specification so that the objection to the disclosure has been overcome, and withdrawal of the objection to the content of the specification is appropriate.

Applicant maintains that the above response provides an adequate clarification to the question presented in the above mentioned prior Office Action "What is '3GIO'?" The above quoted portion of Applicant's disclosure describes 3GIO as a switching fabric technology, along with Rapid I/O<sup>tm</sup>, and HyperTransport<sup>tm</sup>. Persons of ordinary skill in the pertinent art would recognize and understand the term 3GIO.

Further, Applicant respectfully submits that the above referenced previous Office Action merely asked, "What is "3GIO?," and never requested that the Applicant respond to the question of "what this acronym stand for and its importance in the context of this invention."

Serial Number: 10/005,895 Filing Date: November 2, 2001

Title: HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

Assignee: Intel Corporation

However, Applicant maintains that persons skilled in the art would recognize and understand the term 3GIO, and therefore a recitation of the meaning of the "acronym" 3GIO (Applicant does not admit that this is an acronym) is unnecessary for an understanding of the meaning of the term. Further, the Office Action fails to point out a statute, regulation, or a recitation in the Manual of Patent Examining Procedure (MPEP) that forms a basis for a requirement that the Applicant explain the "importance in the context of this invention" of the term 3GIO. Applicant directs attention to 35 U.S.C. § 112 which states in part:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention. (Emphasis added).

Because Applicant believes that the disclosure of the present invention complies with these requirements as set forth in 35 U.S.C. § 112, Applicant respectfully requests withdrawal of the objection to the disclosure of the specification.

# §102 Rejection of the Claims

Claims 1-8, 10-13, 42-49, and 51-58 were rejected under 35 U.S.C. § 102(e) as being anticipated by Walker *et al.* (Ú.S. 6,701,375). Applicant respectfully traverses the rejection of claims 1-8, 10-13, 42-49, and 51-58.

## <u>Applicable Law</u>

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (Emphasis added).

Serial Number: 10/005,895 Filing Date: November 2, 2001

Title: HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

Assignee: Intel Corporation

The Walker et al. reference fails to disclose in a single prior art reference each of the elements in claims 1-8, 10-13, 42-49, and 51-58.

Applicant respectfully submits that the Office Action has failed to establish a *prima facie* case of anticipation in that Walker *et al.* does not disclose each and every element of claims 1-8, 10-13, 42-49, and 51-58 as arranged in the claims.

For example, independent claim 1 recites,

a multi-dimensional switching fabric coupled to said first processing domain and said second processing domain to provide peer-to-peer packet communication within said processing system on multiple orthogonal planes, a first plane providing intra-domain packet communication and a second plane providing inter-domain packet communication. (Emphasis added).

In another example, independent claim 42 recites,

a multi-dimensional switching fabric coupled to each of the plurality of processing subsystems to provide peer-to-peer communication within the system on multiple orthogonal planes, including a first plane providing intra-domain communications, a second plane providing inter-domain communication within each of the plurality of processing subsystems, and a third plane providing communication among the plurality of processing subsystems. (Emphasis added).

In a further example, independent claim 53 recites,

determining whether the information packet is to be transmitted on a first plane or a second plane; and transmitting the information packet on the first plane or the second plane. (Emphasis added).

In contrast, Walker *et al.*, at column 2, lines 55-62 states, "the method of the invention comprises the steps of: using an <u>auxiliary communication channel to establish switched virtual circuit</u> between a first router associated with a first host and a second router associated with a second host; <u>transmitting data packets in both directions over the switched virtual circuit</u>; and deactivating the switched virtual circuit when packet transmission activity has ceased for a selected time." (Emphasis added).

Serial Number: 10/005,895 Filing Date: November 2, 2001

Title: HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

Assignee: Intel Corporation

Hence, Walker et al. fails to disclose "peer-to-peer packet communication within said processing system on multiple orthogonal planes," including a first plane and a second plane, as recited in claim 1. Walker et al. also fails to disclose "peer-to-peer packet communication within the system on multiple orthogonal planes," including a first plane and a second plane and a third plane, as recited in claim 42. Further, Walker et al. discloses transmitting data packets in both directions over a switched virtual circuit, but fails to disclose "determining whether the information packet is to be transmitted on a first plane or a second plane; and transmitting the information packet on the first plane or the second plane," as recited in claim 53.

The Office Action on page 6 in the section labeled Response to Arguments states,

In response it id [sic] stated that "physical structure of a switched or network, such as LAN's are typically connected through switching nodes, refer to col. 1 lines 20-24, and col. 4 lines 34-36". refer to figs 1-3, abstract, (refer to network of interconnected computers (nodes) and techniques for routing messages or data packets from one node to another (intra-domain), and also when nodes are wide apart from local area, col. 1 lines 10-20, 30-35, and 40-46; col. 2 lines 3-4, 50-55, col. 2 line 66 through col. 3 line 1.

Applicant disagrees. Walker et al. at column 1, lines 20-24 states,

LANs are typically interconnected through switching nodes called bridges and routers, to form a large "internet" of interconnected computer nodes.

Further, Walker et al. at column 4, lines 34-37 states,

The wireless networks 10, 12 and 14 each have a plurality of switch nodes or routers 16 connected to them. Each router 16 may be connected to one or more of the networks 10, 12 and 14 and to other networks not shown in the figure.

However, the above quoted portions of Walker *et al.* fail to disclosure the elements included in claims 1, 42, and 53, including but not limited to, multiple orthogonal planes, a first plane, a second plane, a third plane, and determining whether the information packet is to be transmitted on a first plane or a second plane, as included in claims 1, 42, and 53, as quoted above.

Serial Number: 10/005,895 Filing Date: November 2, 2001

Title: HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

Assignee: Intel Corporation

Applicant's representatives fail to find, and the Office Action fails to point out in Walker et al., where these elements included in claims 1, 42, and 53 as quoted above are disclosed in Walker et al. Because Walker et al. fails to disclose each of the elements included in claims 1, 42, and 53, these claims are not anticipated by Walker et al. Therefore, the Office Action fails to state a prima facie case of anticipation with respect to claims 1, 42, and 53, and so the 35 U.S.C. § 102 rejection of claims 1, 42, and 53 cannot stand.

Claims 2-8 and 10-13 depend from claim 1. Claims 43-49 and 51-52 depend from claim 42. Claims 54-58 depend from claim 53. Thus, claims 2-8, 10-13, 43-49, 51-52, and 54-58 include each of the elements recited in the claim from which they depend. For reasons analogous to those stated above with respect to claims 1, 42, and 53, and additional elements recited claims 2-8, 10-13, 43-49, 51-52, and 54-58, dependent claims 2-8, 10-13, 43-49, 51-52, and 54-58 are not anticipated by Walker *et al.* Thus, the Office Action fails to state a *prima facie* case of anticipation with respect to claims 2-8, 10-13, 43-49, 51-52, and 54-58, and so the 35 U.S.C. § 102 rejection of claims 2-8, 10-13, 43-49, 51-52, and 54-58 cannot stand.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the § 102 rejection and reconsideration and allowance of claims 1-8, 10-13, 42-49, and 51-58.

## §103 Rejection of the Claims

Claims 9, 50, and 55 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walker as in claim 1 above, in view of Nabkel *et al.* (U.S. 6,674,725). Applicant respectfully traverses the rejection of claims 9, 50, and 55.

Claim 9 is ultimately dependent upon claim 1, and so claim 9 is patentable over Walker et al. for at least the same reasons as claim 1. Claim 50 is ultimately dependent upon claim 42, and so claim 50 is patentable over Walker et al. for at least the same reasons as claim 42. Claim 55 is ultimately dependent upon claim 53, and so claim 55 is patentable over Walker et al. for at least the same reasons as claim 53.

Further, Nabkel et al. does not supply any elements missing from Walker et al. as to claims 1, 42, and 53. Therefore, neither Walker et al. nor Nabkel et al., either alone or in combination, teach or suggest all of the elements of claims 9, 50, and 55. Thus, the Office Action fails to state a prima facie case of obviousness with respect to claims 9, 50, and 55.

Serial Number: 10/005,895 Filing Date: November 2, 2001

Title: HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

Assignee: Intel Corporation

For at least the reasons stated above, Applicant respectfully requests withdrawal of the §103 rejection and reconsideration and allowance of claims 9, 50, and 55.

## Allowable Subject Matter

The Office Action fails to state a grounds for rejecting claim 59. Therefore, Applicant respectfully requests that the next official communication indicate that claim 59 is allowed.

# Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

Serial Number: 10/005,895 Filing Date: November 2, 2001

Title: HIERARCHICALLY ORTHOGONAL SWITCHING FABRIC

Assignee: Intel Corporation

### Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

OLEG AWSIENKO ET AL.

By their Representatives, SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Attorneys for Intel Corporation P.O. Box 2938 Minneapolis, Minnesota 55402 (612) 349-9592

Date Jan. 3, 2006

Ann M. McCrackin Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3rd day of January, 2006.

Name

Signature